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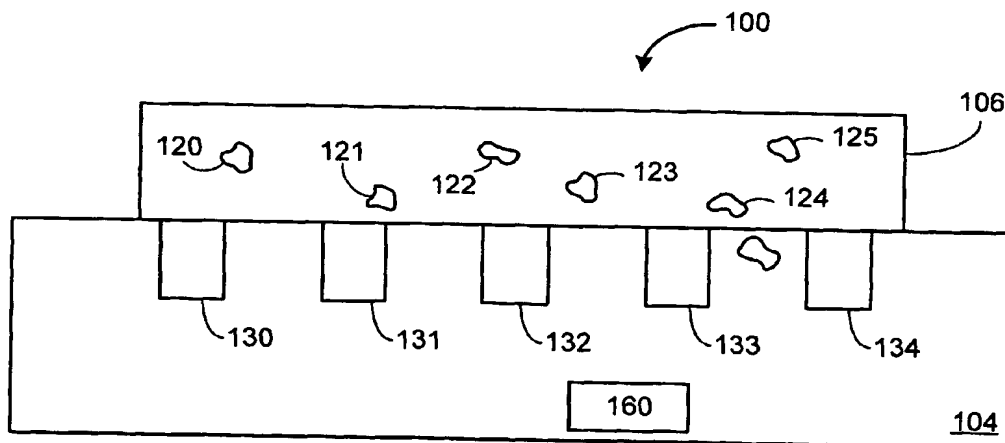
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[Continued on next page]

(54) Title: TAMPER-RESISTANT PACKAGING AND APPROACH



(57) Abstract: A tamper-resistant packaging approach protects non-volatile memory (108). According to an example embodiment of the present invention, a package (106) having a plurality of magnetic particles (120-125) therein is arranged with an integrated circuit device (100) to cause a plurality of magnetically-responsive circuit nodes (130-134) to take on magnetic states. Each magnetic state is detected as a logic state, and then compared with a real-time logic state of the magnetically-responsive circuit nodes and, in response to a stored logic state being different from a real-time logic state, package tampering is detected. In one instance, tampering is removed. The detected tampering may alter a characteristic of the integrated circuit, such as by altering stored data or setting a tamper flag that indicates the package has been tampered with.



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EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)

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C. DOCUMENTS CONSIDERED TO BE RELEVANT

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| Y A | US 2001/033012 A1 (KOEEMERLING OLIVER ET AL) 25 October 2001 (2001-10-25) paragraph '0097! - paragraph '0117! paragraph '0218! - paragraph '0219! | 1, 15, 19 2, 8-14, 16-19 |
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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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